APPLICATION NOTE

LDO Voltage Regulator with Enable Function and low I_Q

About LDO

A low dropout (LDO) voltage regulator is a linear device that maintains a stable output over a wide range of input voltages and output currents. LDOs operate at low voltage differences between input and output. Furthermore, they can be used as noise reduction patches to solve voltage regulation problems caused by electromagnetic interference (EMI) and printed circuit board (PCB) routing. Luckily, the enable function allows switching the regulator on and off, thus improving the overall system efficiency by turning off unused functions.

Enabling

The Enable input (EN), available in positive and negative logic, turns the device on and off by an external signal. Active-high logic activates the device when the voltage at the EN-input exceeds the high-logic threshold. The active-low logic switches the device off when the EN-voltage falls below the logic low threshold. The EN-function is an important feature when sequencing power supplies in multi-rail systems. Keeping the internal bandgap reference running while the regulator is disabled allows for fast turn-on times.

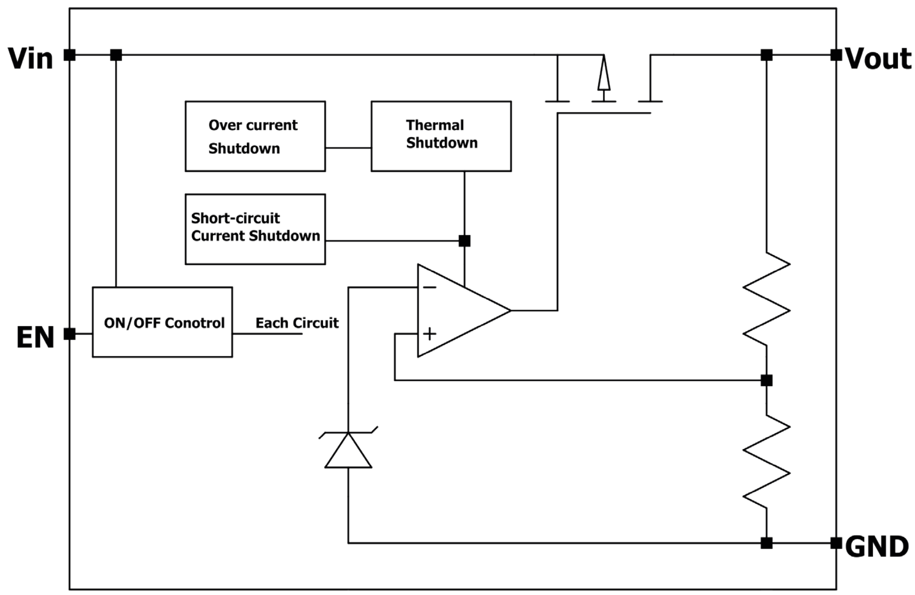

Figure 1: LDI8119-xxEN internal block diagram

Diotec Semiconductor

Shutdown-Current and Quiescent current

When the LDO is turned off and connected to the battery system, the input current will be limited, usually up to 1 µA. This Shutdown current is commonly confused with the quiescent current which is the current drawn by the device when it is enabled and operating with no load. Both shutdown and quiescent current are important parameters when realizing long battery lifetimes in portable devices.
Using the datasheet values for shutdown and quiescent current designers can calculate power dissipation as shown in the below equations.

For example, when the device is fully operational, the voltage is regulated from V_{IN} 10.0 V to V_{OUT} 5.0 V with an output current of 400 mA. The datasheet value for quiescent current is 60 µA. This will result in a power dissipation (P_D) of:

Check again with new value for I_Q

$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} + (V_{IN} \cdot I_Q)$
$P_D = (10\ V - 5\ V) \cdot 0.4\ A + (10\ V \cdot 0.00006\ A)$
$P_D = 2.0006\ W$

When the device is switched into no load operation, the output current falls as low as 200 µA. Then the P_D becomes:

$P_D = (10\ V - 5\ V) \cdot 0.0002\ A + (10\ V \cdot 0.00006\ A)$
$P_D = 1.6\ mW$

In this case, the quiescent current accounts for nearly 50% of the total power dissipation. In conclusion, the following is stated: For applications where the device operates mostly under no load conditions, the quiescent current plays a major role and should be considered when planning the design.

Part no.	Package	Tolerance	Max. Input Voltage V_{IN}	Output Voltage V_{OUT}	Output Current I_{OUT}	Dropout Voltage V_D	Quiescent Current I_Q

LDI8119EN Series

LDI8119-3.3EN	SOT-23-5	2 %	18 V	3.3 V	400 mA	260 mV	60 µA
LDI8119-05EN				5.0 V	400 mA	210 mV	60 µA

LDI8233EN Series *in development*

LDI8233-3.3EN	SOT-23-5	1 %	40 V	3.3 V	100 mA	580 mV	3.5 µA
LDI8233-05EN				5.0 V	100 mA	580 mV	3.5 µA
LDI8233-12EN				12 V	100 mA	580 mV	5.0 µA