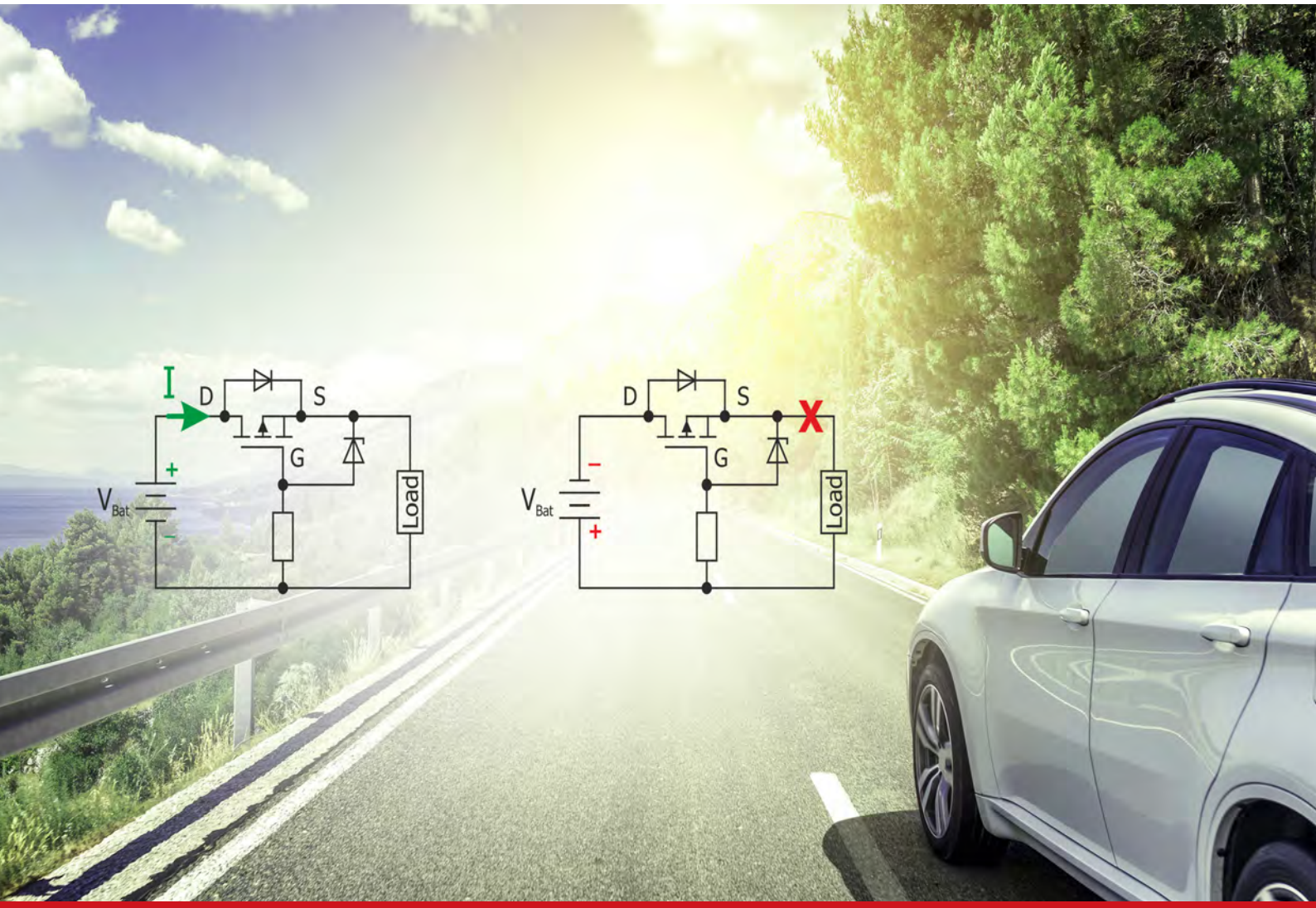
APPLICATION NOTE

Diotec Semiconductor



Automotive Reverse Polarity Protection

Automotive electronic circuits must be protected against negative voltages at the input terminals. Such events can occur during service time or jump start of the vehicle when the battery cables are being connected erroneously. Reverse voltage polarity can cause negative current flow through electronic circuits and a fraction of time under this condition is enough to cause permanent damage to sensors, controllers, and other sensitive silicon components. With this in mind, hardware designers must take appropriate measures to keep automotive electronic control units (ECUs) unharmed after a reverse polarity event. This application note describes three different topologies of reverse polarity protection circuits.

1. Diode in the power path

The simplest method to block negative current flow is a diode in series with the battery. As long as the voltage difference between the diode's anode and cathode is positive and greater than the specified forward voltage (Fig. 1), the diode is forward-biased and current flows into the load circuit. As soon as the battery terminals are swapped (Fig. 2), the diode is reverse-biased and negative current flow is blocked.
When selecting a diode for reverse polarity protection, designers must take into account a few criteria:

- V_F: forward voltage drop across the diode during forward-bias condition. Typical values for standard rectifier diodes are in the range of 0.7V-1.1 V. In order to reduce power dissipation ($V_F \cdot I$) during operation designers may decide to use a Schottky diode, which offers a V_F of lower than 0.5 V. Furthermore, a low V_F will assure more headroom for the downstream circuit during cold crank condition, when the voltage at the power connectors of the ECU can drop to 4 V or lower.

- I_{FAV}: maximum average forward rectified current is the maximum current that the diode is designed to conduct during the forward-bias condition. I_{FAV} must be higher than the maximum load current of the downstream circuit. For reasons of thermal management and longer lifetime, sufficient safety margin must be taken into account.

- V_{DC}: DC blocking voltage is the voltage that the diode is designed to block. V_{DC} will be applied from the diode's cathode to the anode during a reverse polarity event. For this reason, V_{DC} must be higher than the maximum battery voltage expected during the reverse polarity condition.

- Package: most automotive ECUs are manufactured with surface mount (SMD) components. Diotec offers a broad range of standard and Schottky rectifiers in SMD packages. When selecting a package, designers must weigh the board space budget against the thermal characteristics of the package. The parameters R_{thA}/ R_{thT} (thermal resistance junction-to-ambient / junction-to-terminal) in the datasheet will help calculate the temperature increase in the diode based on the forward voltage and the load current.

- T_j: the total device temperature caused by ambient temperature variations and power dissipation must be at all times lower than T_j. The below formula (*) helps calculate the expected T_j for a given ambient temperature T_A.
An efficient thermal connection of the diode to a metal area will facilitate cooling of the diode.

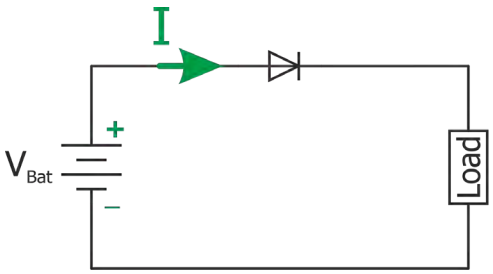


Figure 1

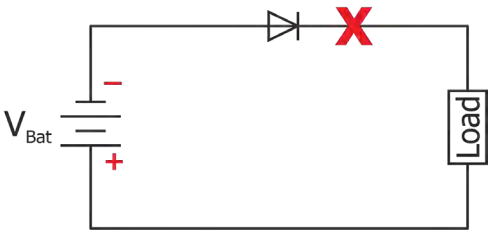


Figure 2

$$T_j = T_A + V_F \times I_{Load} \times R_{thA} \quad (*)$$

+	-
Cost efficient Fast & Easy to design Broad range of types available	Power loss

Part No.	Package	V_F	I_{FAV}	V_{DC}	T_j
SL1D-AQ	SOD-123FL	< 1.1 V	1A	160V	150°C
SKL14-AQ		< 0.55 V	1A	32V	150°C
SKL110-AQ		< 0.85 V	1A	80V	150°C
S2B-AQ	DO-214AA	< 1.15 V	2A	80V	150°C
SK36SMB-AQ		< 0.7 V	3A	48V	150°C
SK56-AQ		< 0.68 V	5A	48V	150°C
S3G-AQ	DO-214AB	< 1.15 V	3A	320V	150°C
SK84-AQ		< 0.5 V	8A	32V	150°C
S1G-AQ	DO-214AC	< 1.1 V	1A	320V	150°C
SK34SMA-3G-AQ		< 0.5 V	3A	32V	150°C
SKL110-AQ		< 0.85 V	1A	80V	150°C
SK110-AQ		< 0.85 V	1A	80V	150°C
SK115-AQ		< 0.85 V	1A	120V	150°C

2. P-FET in the power path

For applications that require high currents or very high efficiency designers can reduce the resistance in the power path by use of a low RDSON P-MOSFET. Connecting the Gate to the Ground will assure a negative V_{GS} voltage that turns the MOSFET ON (Fig. 3). As soon as V_{GS} becomes positive (Fig. 4), the MOSFET will turn off, opening the circuit and thus interrupting current flow.

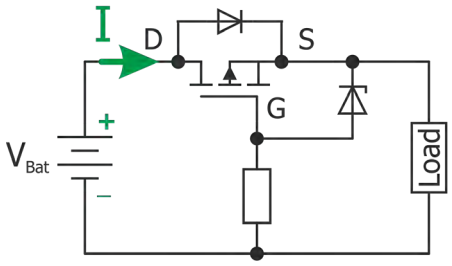


Figure 3

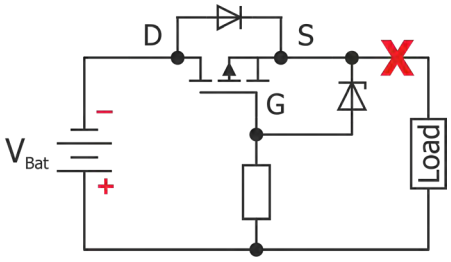


Figure 4

For protecting the circuit against reverse polarity with a P-FET, designers must consider the following parameters:

- $R_{DS(on)}$: Drain-Source On-Resistance is the resistance of the FET during the ON-state. In order to minimize the voltage drop across the FET and reduce power loss during conduction, designers will look for components with a low $R_{DS(on)}$: Being a function of the silicon die area, $R_{DS(on)}$ must be weighed against the FET size and cost.
- V_{DSS}: Drain-Source voltage is the value that the device is designed to withstand when applied between Drain and Source. Its absolute value in the FET datasheet must be greater than the highest expected voltage during the reverse polarity condition.
- I_D: Drain Current must be greater than the maximum load current. With the known value for the load current, designers can calculate the FET conduction losses by using the below formula (**):

$$P_{(Loss,\ cond)} = R_{DS(on)} \times I^2_{Load} \quad (**)$$

+	–
High efficiency	Cost Small range of products

Part No.	Package	V_{DSS}	I_D	$R_{DS(on)}$
DI028P03PT	QFN 3x3	-30 V	-28 A	6.7 mΩ

3. N-FET in the ground path

N-Channel MOSFETs offer a wider variety of products at lower costs than comparable P-Channel FETs. For these reasons, designers may opt for this solution. Due to its internal structure, an N-FET requires a gate voltage VG higher than VDS in order to turn on. Placing the FET in the ground line with the Drain connected to the negative and the Gate to the positive battery terminal will assure current flow through the load (Fig. 5). Once VDS is being pulled over VG during the reverse polarity condition, the FET will turn off thus opening the circuit (Fig. 6). The major drawback in this configuration is the additional resistance in the GND path added by the N-FET's $R_{DS(on)}$, which will alter the GND reference for all other components in the circuit. The same selection criteria as for P-FETs apply in the case of N-FETs.

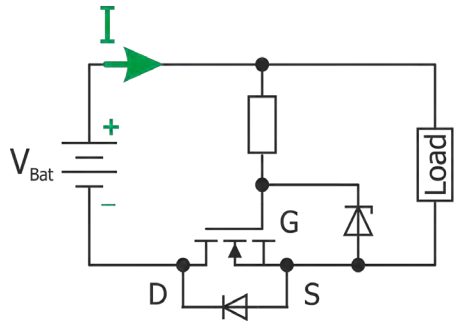


Figure 5

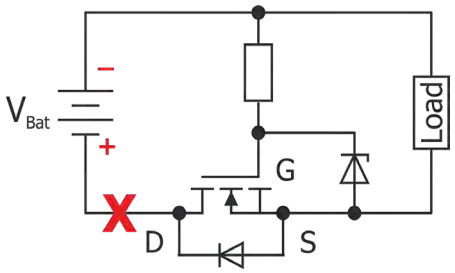


Figure 6

+	–
High efficiency Broad range of types available	Elevated GND Cost

Part No.	Package	V_{DSS}	I_D	$R_{DS(on)}$
DI010N03PW-AQ	QFN 2x2	30 V	10 A	10 mΩ
DI040N03PT-AQ	QFN 3x3	30 V	40 A	6 mΩ
DI045N03PT-AQ		30 V	45 A	3.4 mΩ
DI050N04PT-AQ		40 V	50 A	6.5 mΩ
DI110N04PQ-AQ	QFN 5x6	40 V	110 A	1.9 mΩ
DI068N03PQ-AQ		30 V	68 A	3 mΩ